

PATENT ABSTRACTS OF JAPAN

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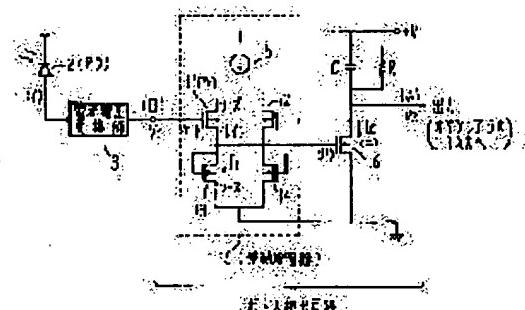
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(21)Application number : **06-097123**(71)Applicant : **FUJITSU LTD**(22)Date of filing : **11.05.1994**(72)Inventor : **CHIBA TAKAYA**
MURAKAMI NORIO**(54) BOTTOM DETECTION CIRCUIT****(57)Abstract:**

PURPOSE: To detect and hold a bottom voltage by adding a positive power supply voltage to a parallel CR circuit with a large time constant at the time of outputting the bottom value of the input signals of an 'L' level from the connection part of one end of a charging circuit and a switching element.

CONSTITUTION: A differential amplifier 10 is formed by connecting the common source of P type MOSFETs 11 and 12 to a constant current source 15 and connecting respective transistors TRs 13 and 14 to the drains of the FETs 11 and 12 as loads and the TRs 13 and 14 are operated as a voltage follower. When the inversion pulses of the 'L' level are inputted to the gate of the FET 11, the FET 11 is turned on, the FET 12 is turned off and a current I₁ is made to flow to the FET 11 and the TR 13. The TR 13 and the TR 16 constituting a current mirror circuit are turned on as well and the discharging current of a capacitor equal to the current I₁ is made to flow to the TR 16. At the time, an output voltage becomes the bottom value 'L' equal to the input signals. Then, when 'H' level signals are inputted to the FET 11 and the time constant of the CR of the parallel circuit of the capacitor and a resistor is defined as a large value, the bottom voltage is detected and held.

**LEGAL STATUS**

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